Module: Logic Design Lab
Name: ……
University no:……..
Group no: ……
Lab Partner Name: *Mr. Mohamed El-Said*

Binary Subtractors

Objective:

- To identify the *half-subtractor* circuit using logic gates and demonstrate its operation.
- To identify the full-*subtractor* circuit using two *half- subtractors* and demonstrate its operation.
- Demonstrate and verify the subtraction operation using *4-bit binary-adder*.

Components Required:

- Mini Digital Logic Trainer.
- IC Type 7404 Hex Inverters.
- IC Type 7408 Quadruple 2-input AND gates.
- IC Type 7432 Quadruple 2-input OR gates.
- IC Type 7486 Quadruple 2-input XOR gates.
- IC Type 7483A 4-bit binary-adder
- Switches for inputs and
- LED displays for outputs.

Theory:

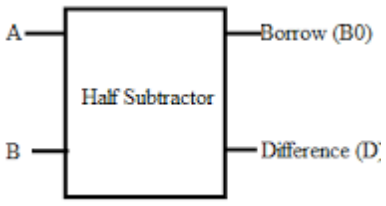
Binary subtraction is performed by two logic circuits *half-subtractor* and *full-subtractor*. Binary *subtraction* can be realized from the following analysis:

Minuend	*A (bit)*
subtrahend	*B (bit)*
Difference	*D (bit)*
Borrow	*B (bit)*

0	-	0	-	1	-	1	-			
0		1		0		1				
0	=	1	=	1	=	0	=			
0		1		0		0				

Half-Subtractor:

A combinational logic circuit that subtract one binary bit **B** from another bit **A**. (A-B) operation produces a difference bit **D** and borrow out bit $\mathbf{B_{out}}$. This logic circuit needs two binary inputs and two binary outputs. The block diagram and truth table of *half-subtractor* circuit as shown in figure 1.



(a)Block diagram

INPUTS		OUTPUTS	
A	B	D	Br
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

(b) Truth table

Figure (1)

From the truth table, the simplified Boolean expressions for the outputs **D** and the $\mathbf{B_{out}}$ is shown as below:

$$D = \overline{A}B + A\overline{B} = A \oplus B$$

$$Bout = \overline{A}B$$

Thus, the logic diagram of half-subtracter circuit is shown in figure (2):

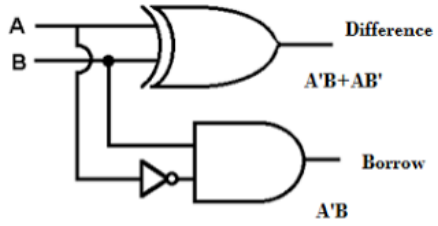
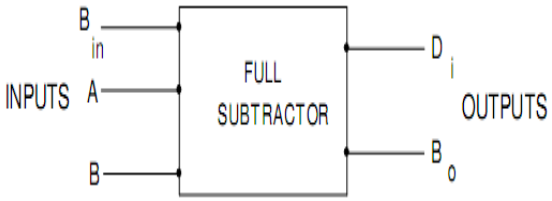


Figure (2) Logic diagram of half-subtractor

Full-Subtractor:

A combinational logic circuit that subtracts three bits, **B** and borrow-in bit $\mathbf{B_{in}}$, (from previous stage) from **A**. Subtraction produces difference bit **D** and borrow out bit $\mathbf{B_{out}}$. Then, this logic circuit needs three binary inputs and two binary outputs. The block diagram and truth table of full-*subtractor* circuit as shown in figure (3).



Input			Output	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

(a)Block diagram (b) Truth table

Figure (3)

From the truth table, the simplified Boolean expressions for the outputs D and the Bout is shown as below:

$$D = \sum m(1,2,4,7) \qquad Bout = \sum m(1,2,3,7)$$

$$D = \overline{A}\,\overline{B}Bin + \overline{A}B\overline{Bin} + A\overline{B}\,\overline{Bn} + ABBin \qquad Bout = \overline{A}\,\overline{B}Bin + \overline{A}B\overline{B}in + \overline{A}BBin + ABBin$$

$$D = (\overline{A}\,\overline{B} + AB)Bin + (\overline{A}B + A\overline{B})\overline{Bin} \qquad Bout = (\overline{A}\,\overline{B} + AB)Bin + (Bin + \overline{Bin})\overline{A}B$$

$$D = \overline{(A \oplus B)}Bin + (A \oplus B)\overline{Bin} \qquad Bout = \overline{(A \oplus B)}Bin + \overline{A}B$$

$$D = (A \oplus B) \oplus Bin$$

So, according the logic expressions for output difference D and output borrow Bout, a full-subtractor is implemented by two half-subtractors and one OR gate as shown in figure (4).

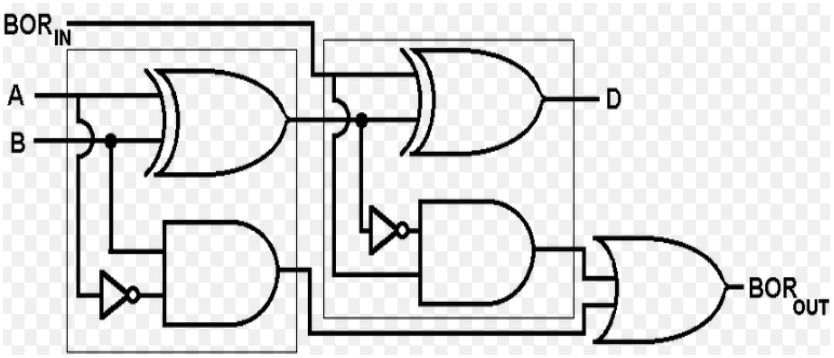


Figure (4) Logic diagram of Full-subtractor

Parallel Adder/Subtractor:

Parallel Add/subtractor is a digital circuit that produces the arithmetic addition / subtraction of two binary numbers. Addition is performed if the control line S=0, while subtraction is performed by adding 2's complement of the subtrahend. (S=1).

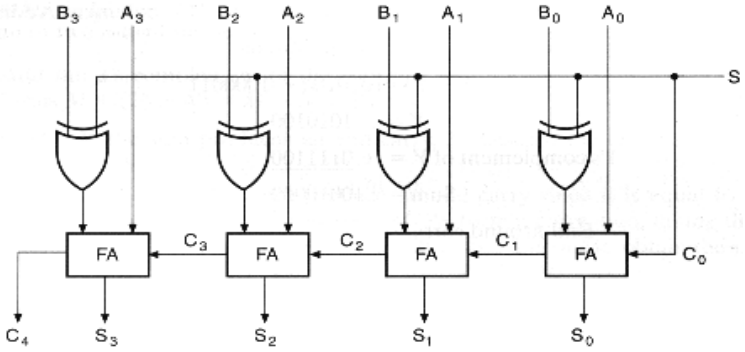


Figure (5) 4-bit binary adder/subtractor circuit

Circuit Operation:

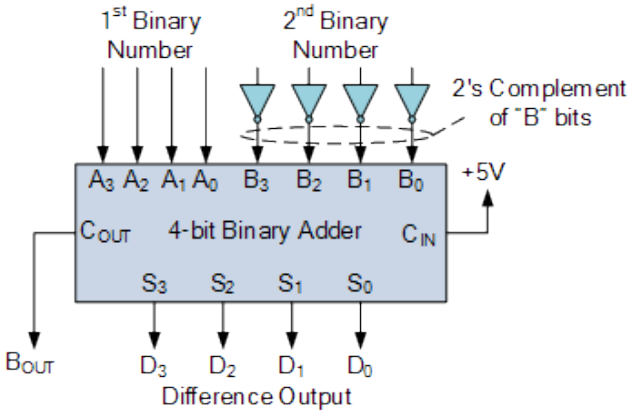
The two numbers are A and B where: $A= A_3A_2A_1A_0$, $B = B_3B_2B_1B_0$

For: **Add operation**, A+B: S=0 and the output of XORs = $B_3B_2B_1B_0$. So, the output is the sum $S_3S_2S_1S_0$ and C_4 denote to the C_{out}.

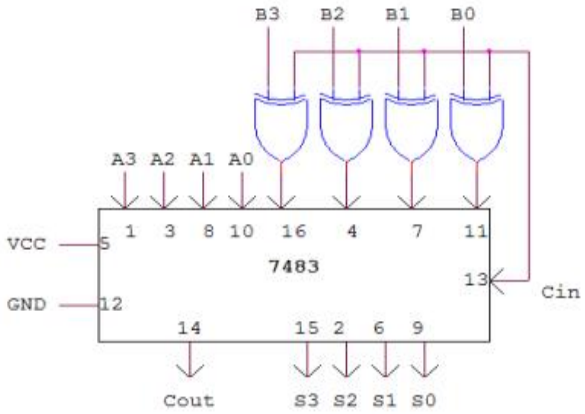
For: **Subtract operation**, A-B: S=1 and the output of XORs = $B_3`B_2`B_1`B_0`$. Then the output is the difference, $D_3D_2D_1D_0$ and C_4 denote to the B_{out}.

Implementation:

The 4-bit binary adder/subtractor circuit is implemented using IC 7483 whose pin diagram is shown in figure (6).



Subtractor Circuit



Adder/Subtractor Circuit

Figure (6)

Part A: Practice Procedure:

- Check the components for their working.
- Connect the circuit diagram in figures (2) and (4).
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram. Verify the Truth Table and observe the outputs.
- Connect the circuit in figure (6) and perform add operation. Find S and C_{out} if A=1110 and B= 1010.
- Repeat to perform subtract operation. Find the difference D and B_{out} if A=1110 and B= 1001.

Results: Binary subtractors are studied.

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<u>Part B:</u> Lab. Exercise:
Students are directed to do the following exercise.

Q1.

a. Explain the Full-subtractor circuit? (write paragraph).
b. Draw the truth table and express the outputs D,Br as minterms.
c. Simplify D,B_{out} using K-map.
d. Draw the logic diagram for D,B_{out} using only basic logic gates.(AND-OR-NOT).
e. How many AND, OR, NOT gates are required to implement the circuit. Name IC's numbers.

Q2.

a. Draw a subtractor circuit to subtract $(10)_2$ - $(6)_2$.
b. Determine the values of bits in A and B.
c. Find the values of bits in the output.

Q3.

a. Draw the 4-bit binary adder-subtractor circuit (Figure 5). Explain operation of the circuit?
b. Let X=1100, Y=101. Find X+Y.
c. Show values for: $S,C_1,C_2,C_3,C_4, S_0, S_1, S_2, S_3, S_4$
d. Use the same circuit to find X-Y. Again repeat **step c**.